REMARKS

Applicants are in receipt of the Office Action mailed January 13, 2006. As indicated above, claim 64 has been added. Therefore, claims 1-64 are pending in the application. Reconsideration is respectfully requested in light of the following remarks.

Objection to the Specification:

The Examiner objected to the title of the application as not descriptive, and stated that a new title clearly indicative of the invention to which the claims are directed is required. The Examiner specifically suggested the title "Processing system with interspersed stall processors and communication elements."

Applicants disagree that the current title of the application fails to clearly indicate the subject matter of the claims. Applicants note that limitations directed to stalling behavior are present only in certain ones of the pending claims reflecting certain ones of Applicants' embodiments. Numerous other pending claims do not specifically recite any aspect of stalling behavior. Broadly speaking, Applicants' claims recite various configurations of systems including interspersed processors and dynamically configurable communication elements, as reflected in the current title. Applicants believe that the present title is descriptive and clearly indicative of the invention to which the claims are directed.

Section 102(b) Rejection:

Claims 1-63 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Wilkinson et al. (U.S. Patent No. 5,805,915) (hereinafter, "Wilkinson"). Applicants traverse this rejection and submit that claims 1-63 as well as newly added claim 64 are not anticipated by, or rendered obvious by, Wilkinson, as set forth in greater detail below.

With respect to claim 1, Wilkinson fails to teach or suggest all of the limitations of Applicants' claim. Specifically, Wilkinson fails to teach or suggest a plurality of dynamically configurable communication elements, each comprising a plurality of communication ports, a first memory, and a routing engine, wherein the plurality of dynamically configurable communication elements are coupled together with a plurality of processors in an interspersed arrangement. Wilkinson further fails to teach or suggest that for each of the processors, a plurality of included processor ports are configured for coupling to a first subset of the plurality of dynamically configurable communication elements, and that for each of the dynamically configurable communication elements, the plurality of communication ports comprise a first subset of communication ports configured for coupling to a subset of the plurality of the processors and a second subset of communication ports configured for coupling to a second subset of the plurality of dynamically configurable communication elements.

As shown in Figures 2 and 4, Wilkinson teaches only a uniform array of interconnected picket processors 100, not an interspersed array of processors and communication elements as recited in claim 1. The Examiner relies on Wilkinson, col. 23, lines 11-16 in asserting that DCC elements are "part of the picket array" of Wilkinson, pointing to col. 22, lines 30-67 in asserting that Wilkinson discloses the communication ports and memory features of the DCC elements of claim 1. Essentially, the Examiner is attempting to argue that each picket 100 of Wilkinson corresponds to both a processor and a communication element of claim 1. However, this interpretation renders the remainder of claim 1 incoherent, in that claim 1 requires that DCC elements have a first subset of communication ports configured for coupling to processors and a second subset of communication ports configured for coupling to other DCC elements. In attempting to show that Wilkinson satisfies this arrangement of connectivity, the Examiner refers to I/O ports 520 discussed at col. 22, lines 30-56 and col. 23, lines 1-16. However, I/O ports 520 have nothing to do with interfacing individual pickets 100 with one another. Rather, Wilkinson clearly discloses that these ports are configured for "communication to associated mainframes or otherwise to the rest of the world," (col. 22, lines 55-56) that is, for communication not among, but external to pickets 100.

Claim 1 requires that a processor including an ALU and an instruction processing unit be configured for coupling, via processor ports, to a subset of DCC elements each including a memory and a routing engine, where DCC elements in turn include ports configured for coupling to processors and other DCC elements. By contrast, Wilkinson discloses a plurality of pickets 100, each including its own memory 102, and each passively connected to one another via propagate and broadcast buses (as shown in Figure 2). Further, while claim 1 clearly requires that DCC elements include a routing engine, it is not clear from the disclosure of Wilkinson that any routing of communications is performed by the pickets themselves. Rather, Wilkinson clearly discloses that execution control of and communication among pickets 100 is controlled by instruction sequencer 402 and execution control 403, which are entirely distinct from and not interspersed among pickets 100 (Figure 4 and col. 20, lines 4-30).

Applicants note that anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. M.P.E.P 2131; *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). The identical invention must be shown in as complete detail as is contained in the claims. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). As Wilkinson discloses dissimilar elements arranged in a fundamentally different fashion compared to Applicants' claim 1, Wilkinson cannot be said to anticipate claim 1.

Applicants also note that Wilkinson fails to teach or suggest the limitations recited in added claim 64. Specifically, Wilkinson fails to teach or suggest that for at least one of the plurality of dynamically configurable communication elements, the first memory includes a plurality of addressable locations and is configured to substantially simultaneously provide a plurality of values stored in the plurality of addressable locations to two or more of the processors. Instead, Wilkinson provides each picket processor 100 with its own respective memory 102, and makes no suggestion whatsoever that a given memory 102 provides data to any entity other than the ALU 101 of the picket

100 in which the given memory 102 is included (Figure 2 and col. 19, lines 50-60). Thus, Applicants submit that added claim 64 is distinguishable over Wilkinson.

Wilkinson further fails to teach or suggest the limitations of independent claim 41. First, as argued above with respect to claim 1, Wilkinson fails to teach or suggest the arrangement of processors and communication elements recited in claim 41. Further, Wilkinson fails to teach or suggest that one of the processors is configurable as a source device to transfer a first plurality of data through an intermediate subset of the plurality of dynamically configurable communication elements to a destination device, wherein, after the source device begins transfer of the first plurality of data through the intermediate subset to the destination device, if either the destination device or one of the intermediate subset stalls, the stalling device is operable to propagate stalling information through one or more of the intermediate subset to the source device, and wherein the source device is operable to suspend transfer of the first plurality of data upon receipt of the stalling information, wherein a portion of the first plurality of data transmitted after the stalling and prior to the suspending is buffered in at least one of the intermediate subset.

The Examiner relies upon col. 19, lines 10-20 of Wilkinson to demonstrate that Wilkinson discloses the stalling behavior recited in claim 41. However, the cited portion of Wilkinson has nothing whatsoever to do with detecting or propagating stall behavior information, or responding to such information in any way. The cited portion refers to a particular example application of Wilkinson's system in which each picket 100 is assigned to model a particular gate or logic function of a digital system (col. 18, lines 62-65). In particular, Wilkinson discloses broadcasting a name and value of a modeled signal to all pickets 100 in response to the modeled signal changing value, whereupon pickets 100 assigned to model gates having input signal names that match the broadcast name receive the changed value and accordingly modify the computed values of the gates (col. 19, lines 1-14). However, the broadcast information is not stalling information; in fact, it does not indicate anything about the operational status of a processor or DCC element at all. Rather, it is information indicative of the value of a logic signal modeled by a picket. Further, upon receipt of a broadcast signal name, Wilkinson does not

suspend transfer of data. Rather, Wilkinson uses the receipt of a signal name as a trigger to capture the value associated with the signal name. As neither the cited portion nor any other portion of Wilkinson disclose the data transfer stalling behavior recited in claim 41, Wilkinson cannot anticipate claim 41. Similar arguments apply to independent claims 43, 45 and 49, each of which recites limitations pertaining to stalling information.

Wilkinson further fails to teach or suggest the limitations of independent claim 52. As argued above with respect to claim 1, Wilkinson fails to teach or suggest processors and dynamically configured communication elements coupled together in an interspersed arrangement. Additionally, Wilkinson fails to teach or suggest that the processors and DCC elements are manufactured on a single integrated circuit, and that each DCC element includes input ports, output registers, and a crossbar, wherein each of the output registers selectively operates in a synchronous data transfer mode or a transparent data transfer mode.

In asserting that Wilkinson teaches that processors and DCC elements are manufactured on a single integrated circuit, the Examiner refers to col. 18, line 56, which refers to one application of the picket system in implementing "checkers for VLSI ground rules violations." However, this refers to a use of Wilkinson's system, and has nothing whatsoever to do with how the system is implemented. In fact, in Figure 5 and at col. 22, lines 6-62, Wilkinson discloses that the picket system is implemented on distinct cards implemented within a rack-mount system, which is precisely the opposite of manufacturing the system on a single integrated circuit.

To support the assertion that Wilkinson discloses that DCC element output registers selectively operate in a synchronous or transparent data transfer mode, the Examiner refers to col. 8, line 64 – col. 9, line 6. However, the referenced section refers broadly to an array processor embodiment in which processors may execute independently of one another and may be synchronized with one another prior to sharing data with one another. Synchronizing independently executing processors simply has nothing to do with a register that selectively operates in a synchronous or transparent data

transfer mode. Moreover, the referenced section of Wilkinson does not describe any embodiment of Wilkinson's system, but rather discusses a completely distinct prior art embodiment. As noted above, anticipation requires disclosure in a prior art reference not only of the elements of a claim, but the arrangement of the elements as recited in the claim. This necessarily includes the recited relationships among elements in the claim. But Wilkinson makes no mention of combining his embodiment with the referenced prior art embodiment in any way. Thus even if, *arguendo*, the combination suggested by the Examiner taught the elements of Applicants' claim, such a combination could not suffice to anticipate Applicants' claim for lack of disclosing their interrelationships.

For at least these reasons, Wilkinson fails to anticipate claim 52. Similar arguments also apply to independent claims 56, 57 and 61, which also recite features relating to devices that operate in a synchronous or transparent data transfer mode. Applicants note that in rejecting claims 57 and 61, the Examiner once again refers to col. 19, lines 10-20, this time asserting that this passage discloses various aspects of synchronous and transparent data transfer recited in Applicants' claims. However, as argued above with respect to claim 41, this section of Wilkinson describes a particular logic circuit modeling application of the picket processor system. It simply has nothing whatsoever to do with data transfer stalling or synchronous or transparent data communication among processors or communication elements.

Wilkinson further fails to teach or suggest the limitations of independent claim 62. As argued above with respect to claim 1, Wilkinson fails to disclose processors and dynamically configurable communication elements configured for coupling as recited in claim 62. Moreover, as argued above with respect to claim 52, Wilkinson does not disclose any aspect of manufacturing such processors and communication elements as an integrated circuit, including fabricating, placing and interconnecting units each comprising a processor and a communication element on a substrate. In fact, as argued above, Wilkinson explicitly discloses that the picket processing system is implemented via discrete components on processor cards within a rack-mount system, which is

precisely contrary to manufacturing of system components on a single substrate as an integrated circuit. Thus, Wilkinson fails to anticipate claim 62.

Wilkinson further fails to teach or suggest the limitations of independent claim 63. As argued above with respect to claims 1 and 62, Wilkinson fails to disclose processors and dynamically configurable communication elements configured for interrelated coupling and manufactured on a single integrated circuit as recited in claim 63. Claim 63 additionally recites that each communication element includes a routing engine configured to route data between any of the communication ports of the communication element, and a direct memory access engine coupled to the communication ports and configured to transfer data between a memory of the communication element and the communication ports.

In rejecting claim 63, the Examiner asserts that col. 15, lines 5-7 and col. 18, lines 7-18 disclose the routing engine and DMA engine features. However, col. 15 merely refers to the distribution of memory among the nodes of a prior art system that is not Wilkinson's embodiment. This has nothing to do with a routing engine configured to route data among ports, and does not amount to a disclosure of a DMA engine of a communication element as recited in Applicants' claim. Even if it did, as argued above with respect to claim 52, a proposed combination of the prior art embodiment with Wilkinson's embodiment could not be said to anticipate claim 63. The cited portion of col. 18 merely refers to an associative memory, which has nothing to do with a DMA engine. Thus, Wilkinson fails to anticipate claim 63.

Applicants further submit that the present claims are not obvious in view of Wilkinson based on the arguments cited above. Applicants additionally note that numerous ones of the dependent claims recite additional distinctions over the cited art. However, as each of the independent claims has been shown to be distinguishable, further discussion of the dependent claims is unnecessary at this time.

CONCLUSION

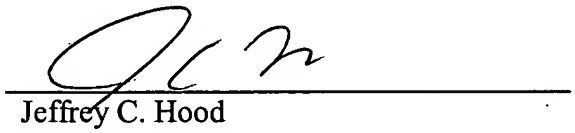
Applicants submit the application is in condition for allowance, and an early notice to that effect is requested.

If any extension of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application from becoming abandoned, Applicants hereby petition for such extension. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 50-1505/5860-00101/JCH.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

Respectfully submitted,



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